CLAIM AMENDMENTS

Please cancel claims 31-33 without prejudice or disclaimer.

Please amend claims 1-2, 4, 9-10, 12, 16-18, 22, 25, 28, and 38 as follows.

1. (Currently Amended) An apparatus, comprising:

a standard hot-plug controller, the standard hot-plug controller having a blinking pattern controller to receive at least one command, the blinking pattern controller to:

cause execution of a first blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus, the first blinking pattern being unique to the command being processed, wherein a first unique blinking pattern is to indicate a first command to turn the indicator "on" solid; and

cause execution of a second unique blinking pattern on the at least one indicator associated with the at least one target peripheral component interconnect slot on the peripheral component interconnect bus, wherein the second unique blinking pattern is to indicate a second command ~~to turn the indicator "off,"~~ different from the first command, wherein the first unique blinking pattern is different from the second unique blinking pattern.

2. (Currently Amended) The apparatus of claim 1, wherein a third unique blinking pattern is to indicate a third command to make the ~~diode~~ indicator blink in a blinking pattern having a duty cycle of approximately fifty percent, and wherein the peripheral component interconnect bus comprises a PCI-Express bus.

3. (Previously Presented) The apparatus of claim 1, wherein a second unique blinking pattern is to indicate a second command to apply power only to at least one target peripheral component interconnect slot, or wherein a third unique blinking pattern is to indicate a third command to enable at least one target peripheral component interconnect slot, or wherein a fourth unique blinking pattern is to indicate a fourth command to disable at least one target peripheral component interconnect slot, or wherein a fifth unique blinking pattern is to indicate a fifth command to change a speed of the peripheral component interconnect bus.

4. (Currently Amended) An apparatus, comprising:

a standard hot-plug controller, the standard hot-plug controller having a blinking pattern controller to receive at least one command, the blinking pattern controller to:

cause execution of a first unique blinking pattern and a second unique blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus, and

the first unique blinking pattern to indicate a hard error occurring during processing of the command and the second unique blinking pattern to indicate a soft error occurring during processing of the command.

5. (Previously Presented) The apparatus of claim 4, wherein the first unique blinking pattern is to indicate an error occurring before power is applied to the target slot.

6. (Canceled).

7. (Previously Presented) The apparatus of claim 4, further comprising a third unique blinking pattern is to indicate an error occurring after power is applied to the target slot.

8. (Previously Presented) The apparatus of claim 4, wherein the unique blinking pattern has a duty cycle that is less than or greater than approximately fifty percent and wherein the peripheral component interconnect bus comprises a PCI-X bus.

9. (Currently Amended) A method, comprising:

receiving a command at a standard hot-plug controller from a microprocessor; and

causing execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus,

the blinking pattern indicating the command being processed,

the blinking pattern having a duty cycle that is ~~less than or greater than approximately~~ not fifty percent ±5%.

10. (Currently Amended) The method of claim 9, further comprising receiving a command to turn the indicator "on," "off," or make the ~~diode~~ indicator blink in a blinking pattern having a duty cycle of approximately fifty percent.

11. (Previously Presented) The method of claim 9, further comprising receiving a command to apply power to the target peripheral component interconnect slot, to enable the target peripheral component interconnect slot, to disable the target peripheral component interconnect slot, or to change the speed of the peripheral component interconnect bus.

12. (Currently Amended) A method, comprising:

causing execution of a first unique blinking pattern and a second unique blinking pattern on at least one indicator associated with at least one target peripheral [card] component interconnect slot on a peripheral component interconnect bus,

the first unique blinking pattern indicating a hard error occurring during processing of the command and the second unique blinking pattern to indicate a soft error occurring during processing of the command.

13. (Previously Presented) The method of claim 12, wherein the first unique blinking pattern is indicating an error occurring before power is applied to the target slot.

14. (Canceled).

15. (Previously Presented) The method of claim 12, wherein the first unique blinking pattern is indicating an error occurring after power is applied to the target slot.

16. (Currently Amended) The method of claim 12, further comprising causing execution of a third unique blinking pattern, the third unique blinking pattern having a duty cycle that is ~~less than or greater than approximately~~ not fifty percent ±5%.

17. (Currently Amended) An article of manufacture including a machine-accessible tangible storage medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving a command at a standard hot-plug controller from a microprocessor; and

causing execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus,

the blinking pattern indicating the command being processed,

the blinking pattern having a duty cycle that is ~~less than or greater than approximately~~ not fifty percent ±5%.

18. (Currently Amended) The article of manufacture of claim 17, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising receiving a command to turn the indicator "on," "off," or make the ~~diode~~ indicator blink in a blinking pattern having a duty cycle of approximately fifty percent.

19. (Previously Presented) The article of manufacture of claim 17, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising receiving a command to apply power to the target peripheral component interconnect slot, to enable the target peripheral component interconnect slot, to disable the target peripheral component interconnect slot, or to change the speed of the peripheral component interconnect bus.

20. (Previously Presented) An article of manufacture including a machine-accessible tangible storage medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving at least one command at a standard hot-plug controller from a microprocessor; and

causing execution of unique blinking patterns on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus, and

the unique blinking patterns indicating unique errors occurring during processing of the command, wherein the unique blinking patterns are to indicate a hard error and/or a soft error occurring during processing of the command.

21. (Previously Presented) The article of manufacture of claim 20, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising indicating an error occurring before power is applied to the target slot.

22. (Currently Amended) The article of manufacture of claim 20, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising causing execution of the blinking pattern at a duty cycle that is ~~less than or greater than approximately~~ not fifty percent.

23. (Previously Presented) The article of manufacture of claim 20, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising indicating an error occurring after power is applied to the target slot.

24. (Canceled).

25. (Currently Amended) A system, comprising:

a peripheral component interconnect bus having at least one peripheral component interconnect slot thereon, the peripheral component interconnect slot having at least one indicator associated therewith,

a bridge coupled to the peripheral component interconnect bus, the bridge having a standard hot-plug controller coupled to the peripheral component interconnect bus, the standard hot-plug controller to receive a command, and cause execution of a blinking pattern on at least one indicator, the blinking pattern to indicate the command being processed, the blinking pattern having a duty cycle that is ~~less than or greater than approximately~~ not fifty percent ±5%.

26. (Original) The system of claim 25, further comprising a memory coupled to the bridge.

27. (Original) The system of claim 26, wherein the memory is a static random access memory (SRAM).

28. (Currently Amended) A system, comprising:

a peripheral component interconnect bus having at least one peripheral component interconnect slot thereon, the peripheral component interconnect slot having at least one indicator associated therewith,

a bridge coupled to the peripheral component interconnect bus, the bridge having a standard hot-plug controller coupled to the peripheral component interconnect bus, the standard hot-plug controller to receive a command, and cause execution of a blinking pattern on at least one indicator, the blinking pattern to indicate an error occurring during processing of the command, the of blinking pattern having a duty cycle that is ~~less than or greater than approximately~~ not fifty percent ±5%.

29. (Original) The system of claim 28, further comprising a memory coupled to the bridge.

30. (Original) The system of claim 29, wherein the memory is a static random access memory (SRAM).

Claims 31-33. (Canceled).

34. (Currently Amended) A system, comprising:

a chipset including:

a standard hot-plug controller having a blinking pattern controller to receive at least one command, the blinking pattern controller to cause execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus, the blinking pattern being unique to the command being processed, wherein a first unique blinking pattern is to indicate a first command to turn the indicator "on" solid, wherein a second unique blinking pattern is to indicate a second command different from the first command, wherein the first unique blinking pattern is different from the second unique blinking pattern; and

static random access memory (SRAM) coupled to the standard hot-plug controller.

35. (Previously Presented) The system of claim 34, wherein the second unique blinking pattern is to indicate a second command to apply power to the target peripheral component slot.

36. (Previously Presented) The system of claim 34, wherein the second unique blinking pattern is to indicate a second command to disable the target peripheral component interconnect slot.